HIGH-VOLTAGE VERTICAL TRANSISTOR WITH EDGE TERMINATION STRUCTURE

RELATED APPLICATIONS

This is a continuation-in-part (CIP) application of application Ser. No. 10/393,759 filed Mar. 21, 2003, which is a continuation of Ser. No. 09/948,930 filed Sep. 7, 2001, now U.S. Pat. No. 6,573,558, both of which are assigned to the assignee of the present CIP application.

FIELD OF THE INVENTION

The present invention relates to semiconductor devices fabricated in a silicon substrate. More specifically, the present invention relates to field-effect semiconductor transistor structures capable of withstanding high voltages.

BACKGROUND OF THE INVENTION

High-voltage, field-effect transistors (HVFETs) are well known in the semiconductor arts. Most often, HVFETs comprise a device structure that includes an extended drain region that supports the applied high-voltage when the device is in the "off" state. HVFETs of this type are commonly used in power conversion applications such as AC/DC converters for offline power supplies, motor controls, and so on. These devices can be switched at high voltages and achieve a high blocking voltage in the off state while minimizing the resistance to current flow in the "on" state. The blocking or breakdown voltage is generally denoted as Vbd. The acronym Rsp refers to the product of the resistance and surface area, and is generally used to describe the on-state performance of the device. An example of a prior art HVFET having an extended drain region with a top layer of a conductivity type opposite that of the extended drain region is found in U.S. Pat. No. 4,811,075.

In a conventional HVFET the extended drain region is usually lightly doped to support high voltages applied to the drain when the device is off. The length of the extended drain region is also increased to spread the electric field over a larger area so the device can sustain higher voltages. However, when the device is on (i.e., conducting) current flows through the extended drain region. The combined decrease in doping and increase in length of the extended drain region therefore have the deleterious effect on the on-state performance of the device, as both cause an increase in on-state resistance. In other words, conventional high-voltage FET designs are characterized by a trade-off between Vbd and Rsp.

To provide a quantitative example, a typical prior art vertical HVFET (NMOS-type) may have a Vbd of 600V with a Rsp of about 16 ohm-mm^2. Increasing the length of the extended drain would affect device performance by increasing Vbd beyond 600V at the expense of a higher Rsp value. Conversely, reducing the length of the extended drain would improve the on-state resistance to a value below 16 ohm-mm^2, but such a change in the device structure would also cause Vbd to be reduced to less than 600V.

A device structure for supporting higher Vbd voltages with a low Rsp value is disclosed in U.S. Pat. Nos. 4,754,310, 5,438,215, and also in the article entitled, "*Theory of Semiconductor Superjunction Devices*" by T. Fujihira, Jpn. J. Appl. Phys., Vol. 36, pp. 6254-6262, October 1977. In this device structure the extended drain region comprises alternating layers of semiconductor material having opposite conductivity types, e.g., PNPNP . . . . As high voltage is applied to the layers of one conductivity type, all of the layers are mutually depleted of charge carriers. This permits a high Vbd at much higher conducting layer doping concentrations as compared to single layer devices. The higher doping concentrations, of course, advantageously lower the Rsp of the transistor device. For example, in the article entitled, "*A new generation of high voltage MOSFETs breaks the limit line of silicon*" by G. Deboy et al., IEDM tech. Digest, pp. 683-685, 1998, the authors report a vertical NMOS device with a Vbd of 600V and a Rsp of about 4 ohm-mm^2.

Another approach to the problem of achieving high-voltage capability is disclosed in the paper, "*Realization of High Breakdown Voltage in Thin SOI Devices*" by S. Merchant et al., Proc. Intl. Symp. on Power Devices and ICs, pp. 31-35, 1991. This paper teaches an extended drain region that comprises a thin layer of silicon situated on top of a buried oxide layer disposed on top of a semiconductor substrate. In operation, the underlying silicon substrate depletes charge from the thin silicon layer at high voltages. The authors claim that high values of Vbd are obtained as long as the top silicon layer is sufficiently thin and the buried oxide layer is sufficiently thick. For instance, a lateral NMOS device with Vbd of 600V and Rsp of about 8 ohm-mm^2 is obtained using this approach.

Other background references of possible interest to those skilled in the art include U.S. Pat. Nos. 6,184,555, 6,191,447, 6,075,259, 5,998,833, 5,637,898, International Application No. PCT/IB98/02060 (International Publication No. WO 99/34449), and the article, "*High Performance 600V Smart Power Technology Based on Thin Layer Silicon-on-Insulator*" by T. Letavic et al., Proc. ISPSD, pp. 49-52, 1997.

Another problem associated with conventional HVFET designs is that they usually require a wide perimeter or edge termination area in order to support the large electric fields developed between the various regions. By way of example, a conventional HVFET design may require an edge termination area in a range of 200 μm-300 μm wide for a 600V device. Naturally, this wide edge termination area uses valuable silicon area leading to increased production costs.

What is needed, therefore, is an improved high-voltage transistor structure that achieves a high Vbd with relatively low on-state resistance while also minimizing the edge termination area that separates the active device cells from the perimeter area.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not limitation, in the figures of the accompanying drawings, wherein:

FIG. **1** is a cross-sectional side view of a vertical high-voltage, field-effect transistor (HVFET) device structure in accordance with one embodiment of the present invention.

FIG. **2** is a cross-sectional side view of one embodiment of a lateral HVFET fabricated in accordance with the present invention.

FIG. **3**A is a top view of lateral HVFET fabricated in accordance with another embodiment of the present invention.

FIG. **3**B is a cross-sectional side view of the lateral HVFET shown in FIG. **3**A, taken along cut lines A-A'.

FIG. **4** is a cross-sectional side view of another embodiment of a vertical HVFET device structure fabricated according to the present invention.

FIGS. **5**A-**5**K are cross-sectional side views of a vertical HVFET device structure taken at various stages in a fabrication process in accordance with yet another embodiment of the present invention.